Overview of Optical Metrology for Ultra-thin Oxide and High-K Gate Dielectrics

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International SEMATECH

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OUTLINE:

1. Current Gate Dielectric Metrology Challenges

2. Implementation of Spectroscopic Ellipsometry to High K/ Ultrathin Oxide Stacked Gate Dielectric Metrology

3. Characterization of Gate Oxide on Silicon-On-Insulator substrates

4. Future Gate Stack Metrology Challenges

1. Current Gate Dielectric Metrology Challenges:

High K gate dielectric films exhibit sensitive dependence on material composition— need to control material composition

Also High K may be stacked on Ultra-thin Oxide interface to preserve channel mobility— need to control interfacial thickness in "EOT" measurement

Review paper: G.D. Wilk, R.M. Wallace, J.M. Anthony, "High K gate dielectrics: current status and materials properties considerations", J. Appl. Phys., vol. 89, 5243 (2001).

Gate Oxide Metrology:

$$\frac{1}{C_{total}} = \frac{1}{C_{oxide}} + \frac{1}{C_{pd}} + \frac{1}{C_{inv}}$$

Relies on correlation of physical thickness of oxide and device electrical thickness

$$C = \frac{\varepsilon \times A}{t} \qquad CET = EOT + offset$$

$$"y = mx + b" \qquad EOT = 3.92 \times T_{oxide}$$

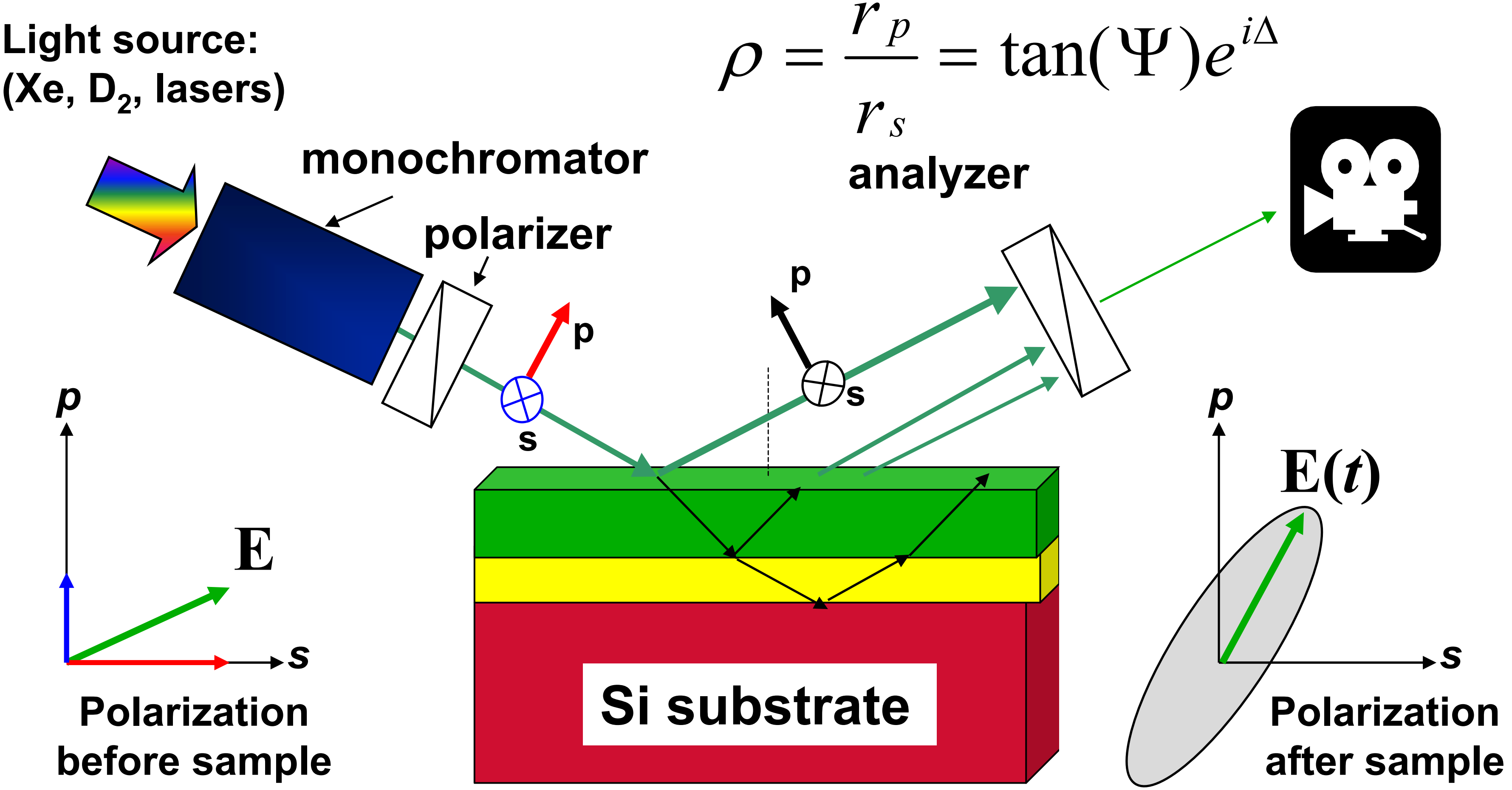
- **Poly-depletion and inversion layer capacitance treated as fixed offset**

Clive Hayzelden, "Gate Dielectric Metrology", in *Handbook of Silicon Semiconductor Metrology,* edited by Alain C. Diebold, pp. 17-47 (Marcel-Dekker, New York, 2001).

Ellipsometry for Gate Dielectric Metrology:

- Ellipsometric thickness measurement provides acceptable precision for Gate Oxide
- However, high K stack is more complex…

$$\rho = \frac{r_p}{r_s} = \tan(\Psi)e^{i\Delta}$$



Ellipsometric approach for High K gate dielectric metrology:

"Ideal" high K ⇒ $$EOT = \frac{\varepsilon_{oxide}}{\varepsilon_{highK}} \times T_{highK}$$

If dielectric constant of film is known, then only need high K film physical thickness— conclusion in this case is that ellipsometric approach will work

However, high k composition has proven notoriously difficult to control in practice ⇒ now must also track high K film material properties in ellipsometric approach

Need to limit number of fit parameters
⇒ improved precision

Need appropriate dispersion functional form ($\varepsilon_2 \neq 0$)
⇒ improved precision

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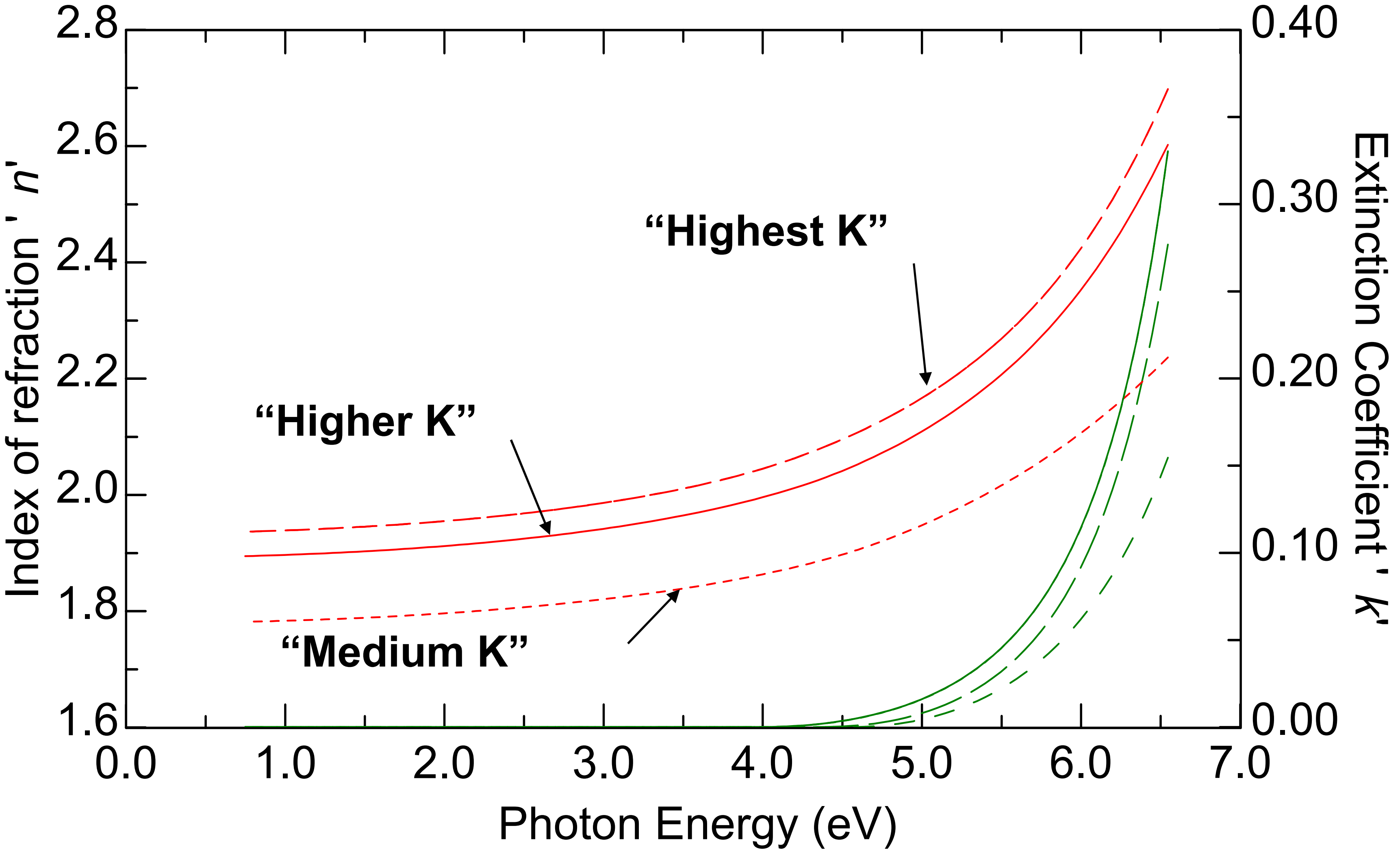
Typical optical response of Hi-K films:



- **Index tracks K value— normally will exhibit approximate linearity over process range**

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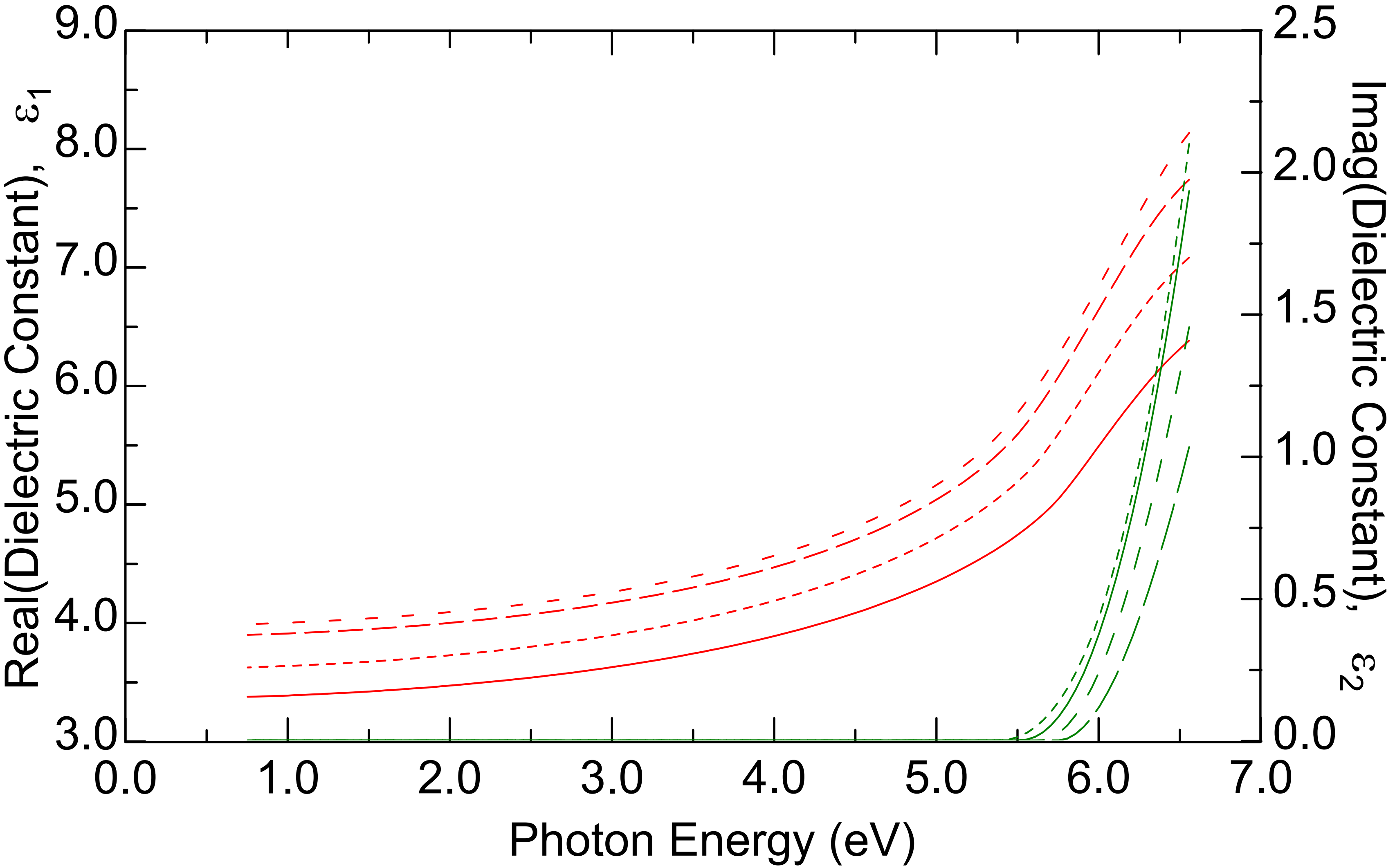
ALCVD High K alloy dielectric functions: Optical Constants



- **Tauc-Lorentz Optical models**

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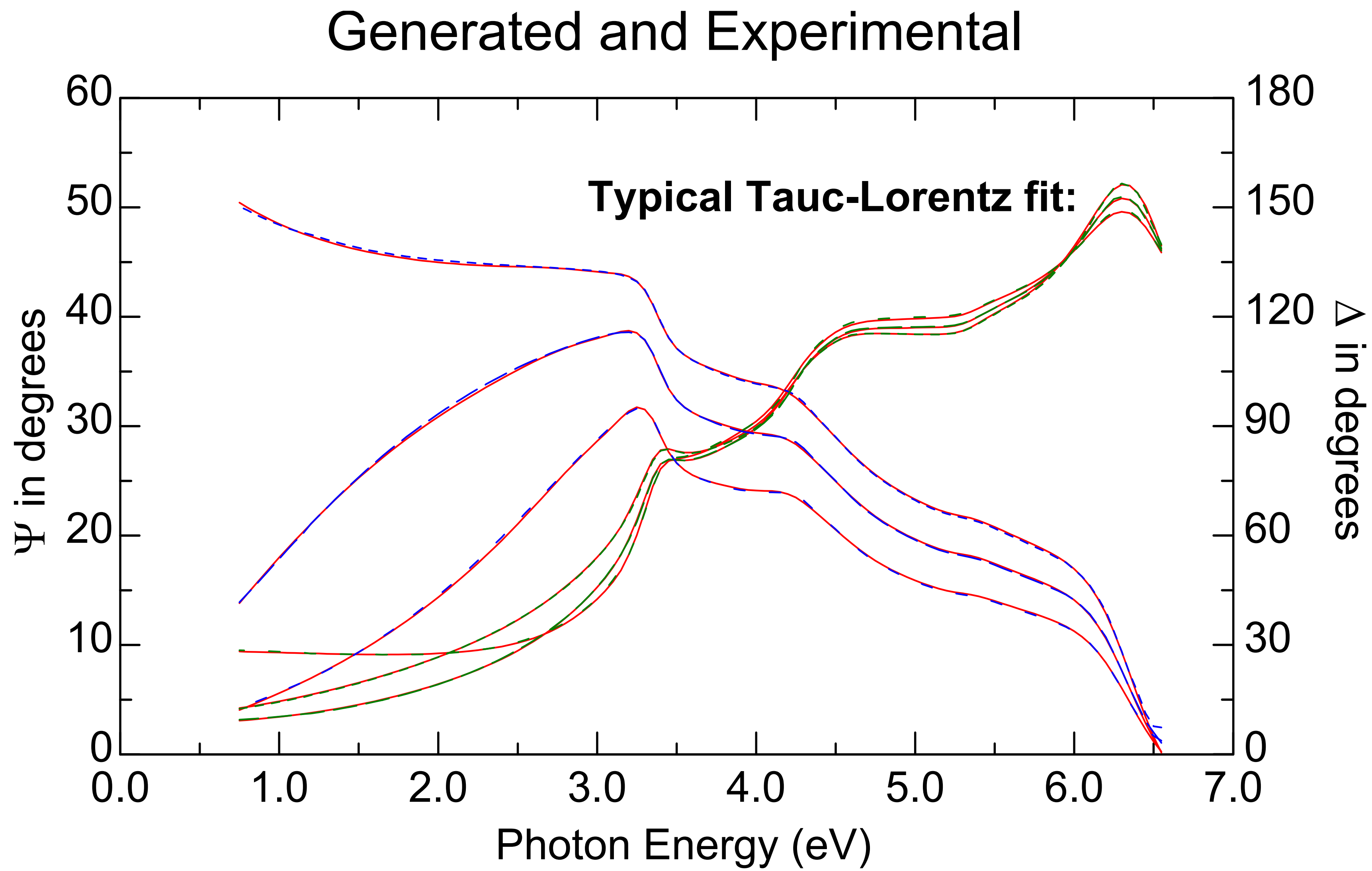
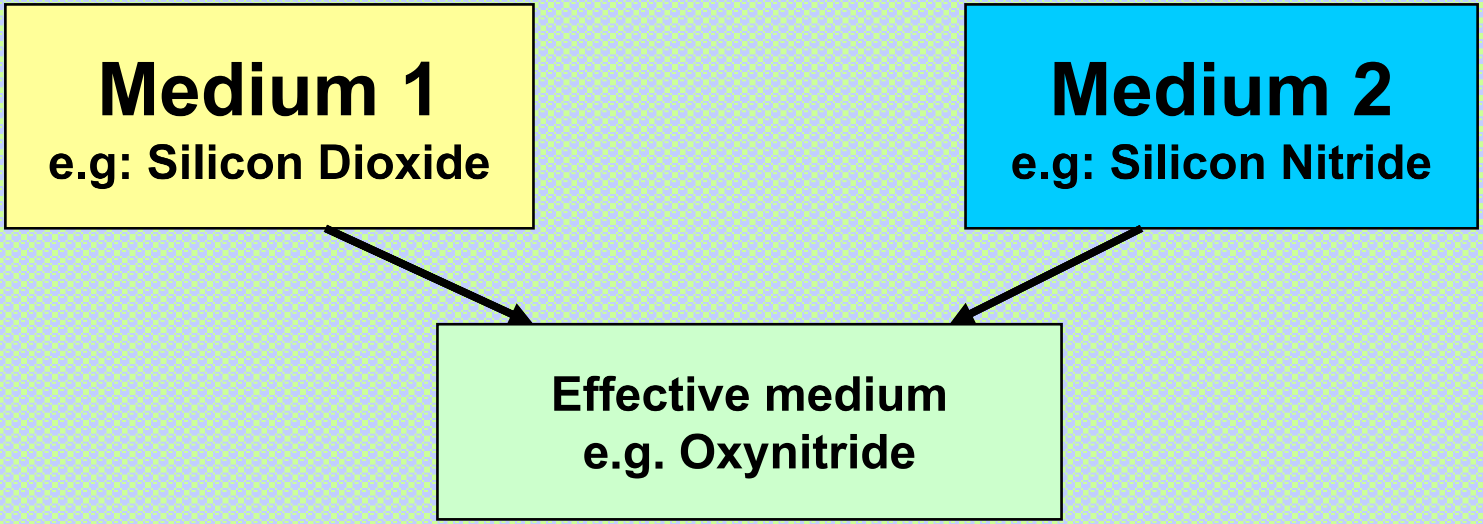
Spectroscopic Ellipsometry of ALCVD High K alloys



Effective medium approach:



Medium 1
e.g: Silicon Dioxide

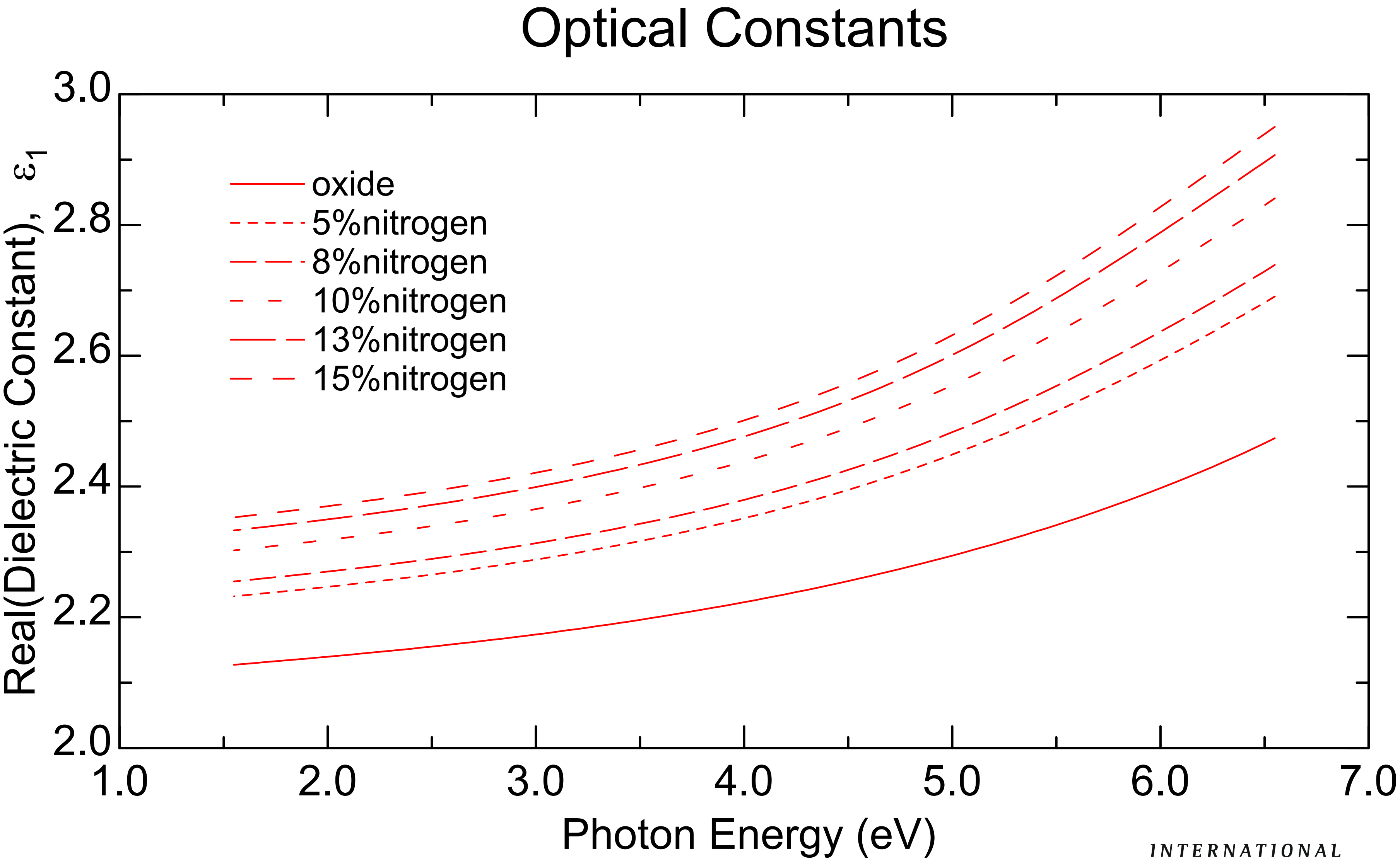
Medium 2
e.g: Silicon Nitride

Effective medium
e.g. Oxynitride

Advantages

- may combine known material dispersions
- allows calibration to material composition

Nitrogen content determination in oxynitrides via spectroscopic ellipsometry:



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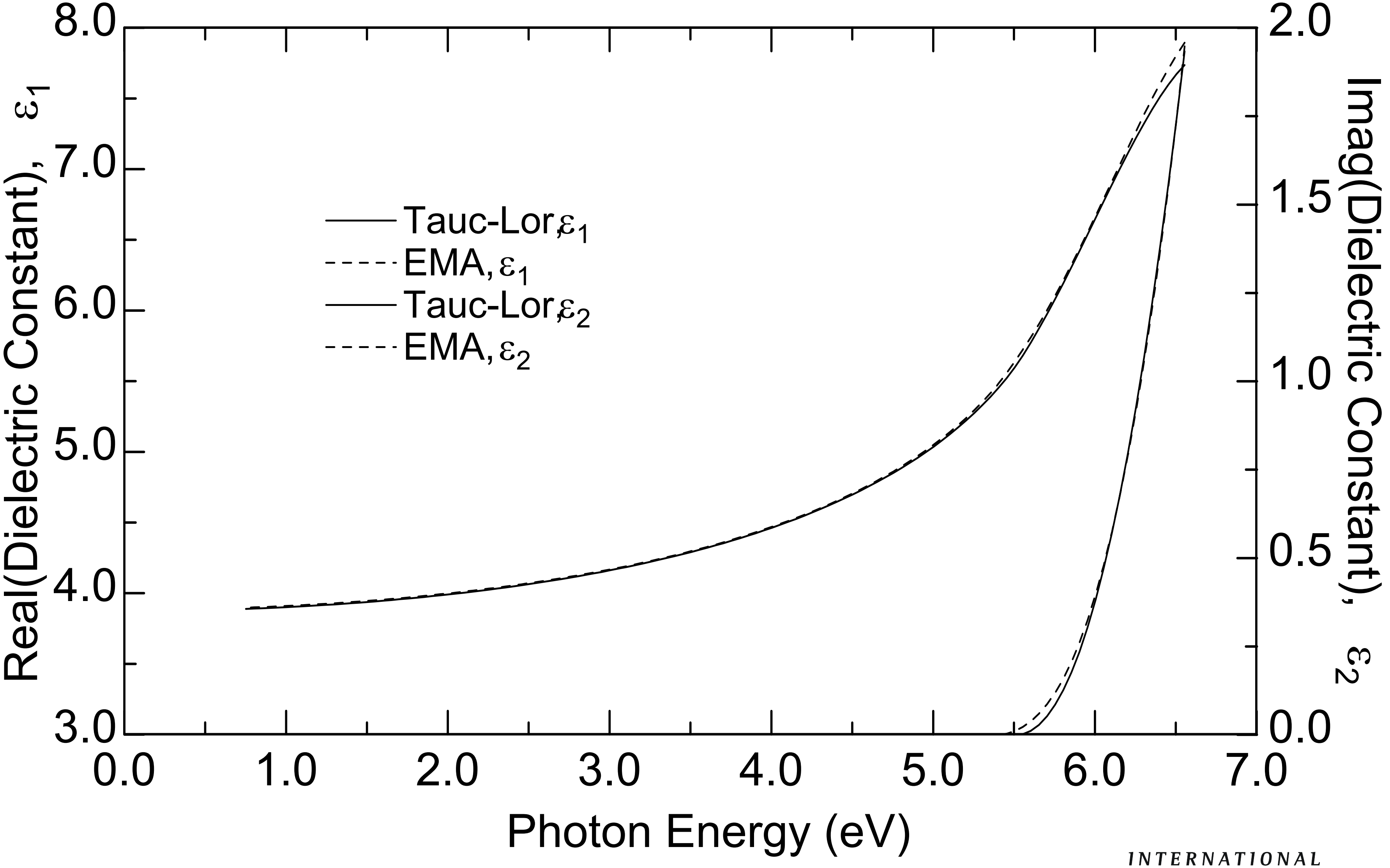
EMA with Tauc-Lorentz constituents for fitting High K process window:



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High-K Gate Dielectric Metrology:

Real High K has ultra-thin interfacial oxide ⇒

Potentially Requires:

1. Hi-K film physical thickness
2. K value
3. Interfacial oxide thickness

$$EOT = \frac{\kappa_{oxide}}{\kappa_{highK}} \times T_{highK} + T_{oxide}$$

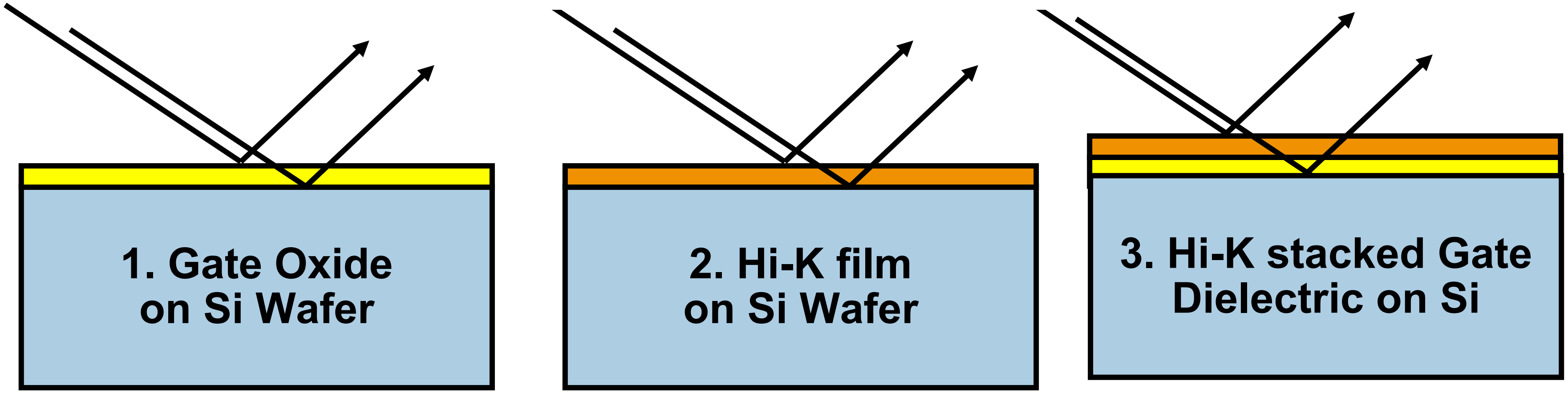
Reduced correlation to device performance

Will SE work for Ultra-thin Oxide layers below high K?

- Ellipsometry: sensitive to "total" dielectric physical thickness, but limited sensitivity to interfacial thickness

Gate Dielectric Modeling Approach:

1. Gate Oxide- Single Wavelength Ellipsometry (laser based) for $T_{ox} \Rightarrow$ acceptable "EOT" precision
2. "Ideal" High K- Spectroscopic Ellipsometry (lamp based) for material content and $T_{hi\text{-}K}$, $\Rightarrow$ precision too large by ~4x
3. High K/ Ultra-thin Oxide Stack- No Best Known Method established to date



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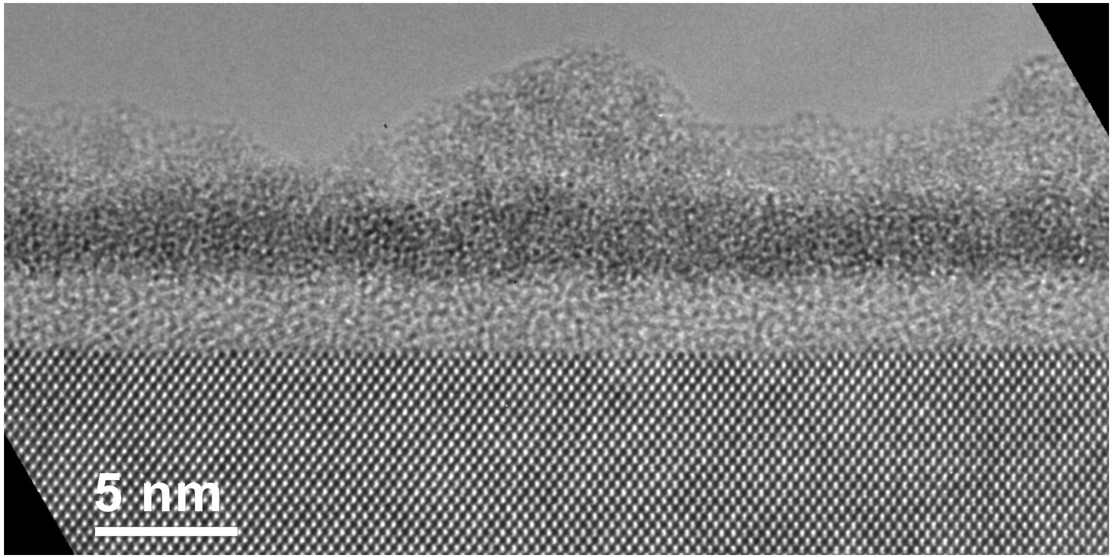
Hi-K/ Interfacial Oxide Stacked for SE Calibration:

A. High K silicates with Ultra-thin interface ~5A: 2 high K compositions with & w/o Post Deposition Anneal— 4 wafers

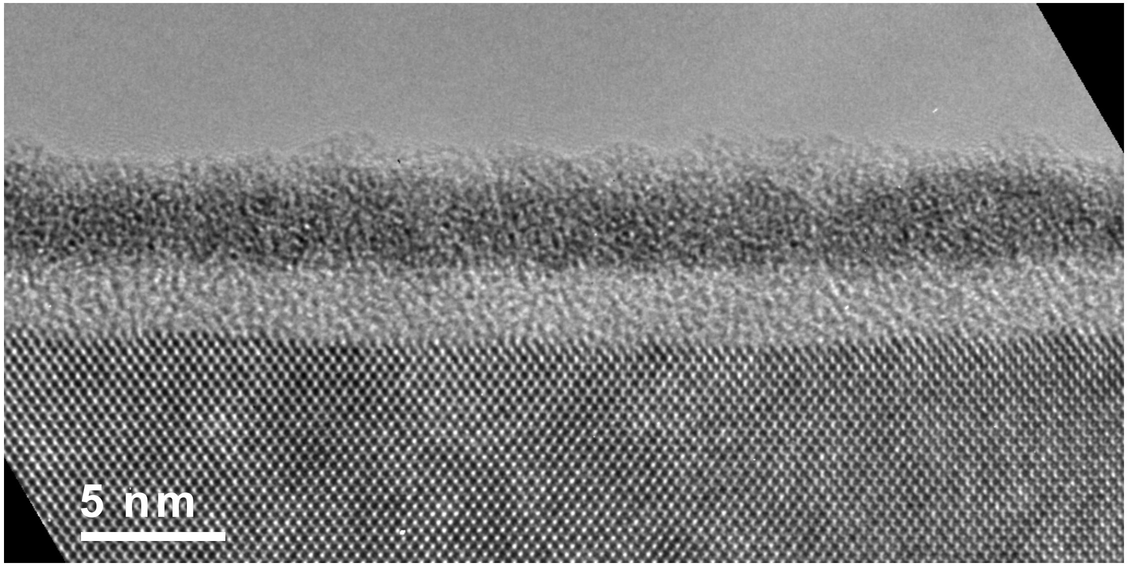
B. High- K silicates with Rapid Thermal Oxide underlayer ~25 A: 2 high K compositions with & w/o PDA— 4 wafers

C. High- K silicates with Rapid Thermal Oxide underlayer ~20 A: 2 high K compositions with & w/o PDA— 4 wafers

HRTEM— Hi-K #2/ Oxide #1



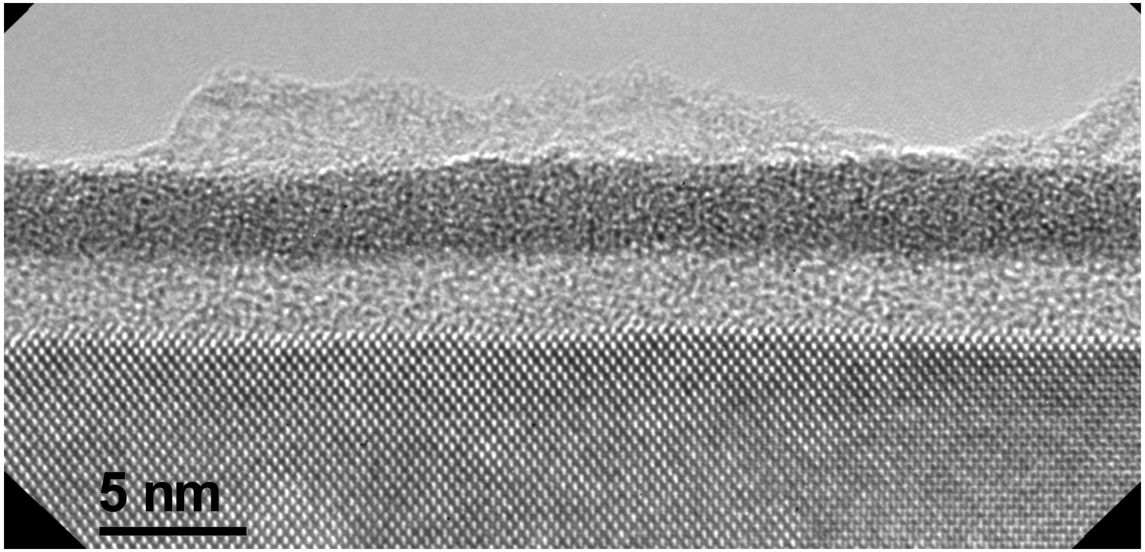
2.7 – 3.3 nm high-k
2.3 nm SiO2



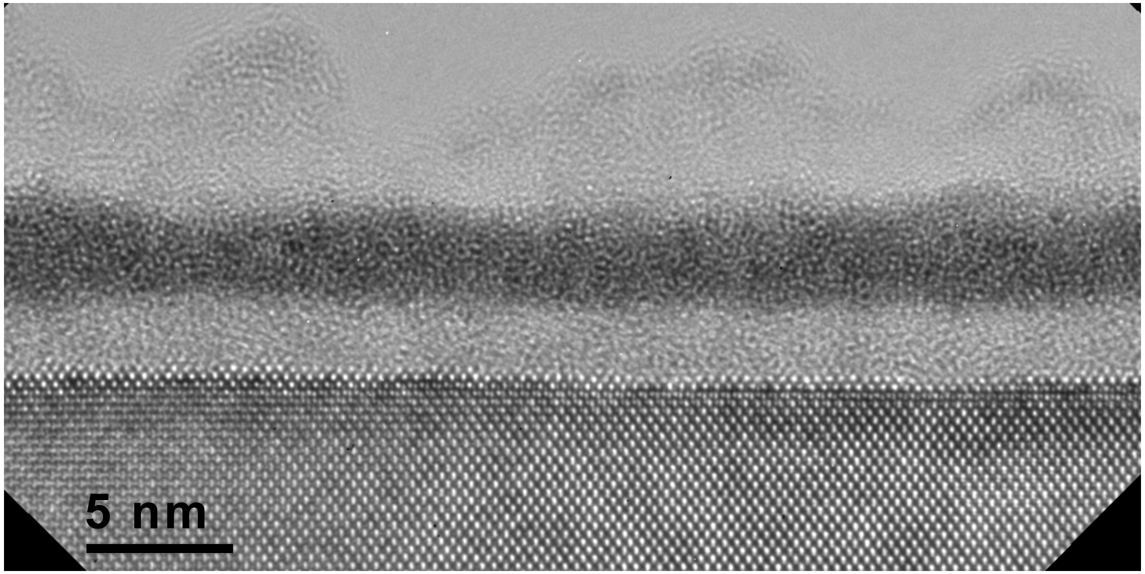
2.9 – 3.4 nm high-k
2.0 – 2.3 nm SiO2

Courtesy Brendan Foran, ISMT

HRTEM— Hi-K #1/ Oxide #2 with Post Deposition Anneal



3.2 – 3.6 nm high-k
2.3 nm SiO2



3.3 – 3.7 nm high-k
2.0 – 2.2 nm SiO2

Courtesy Brendan Foran, ISMT

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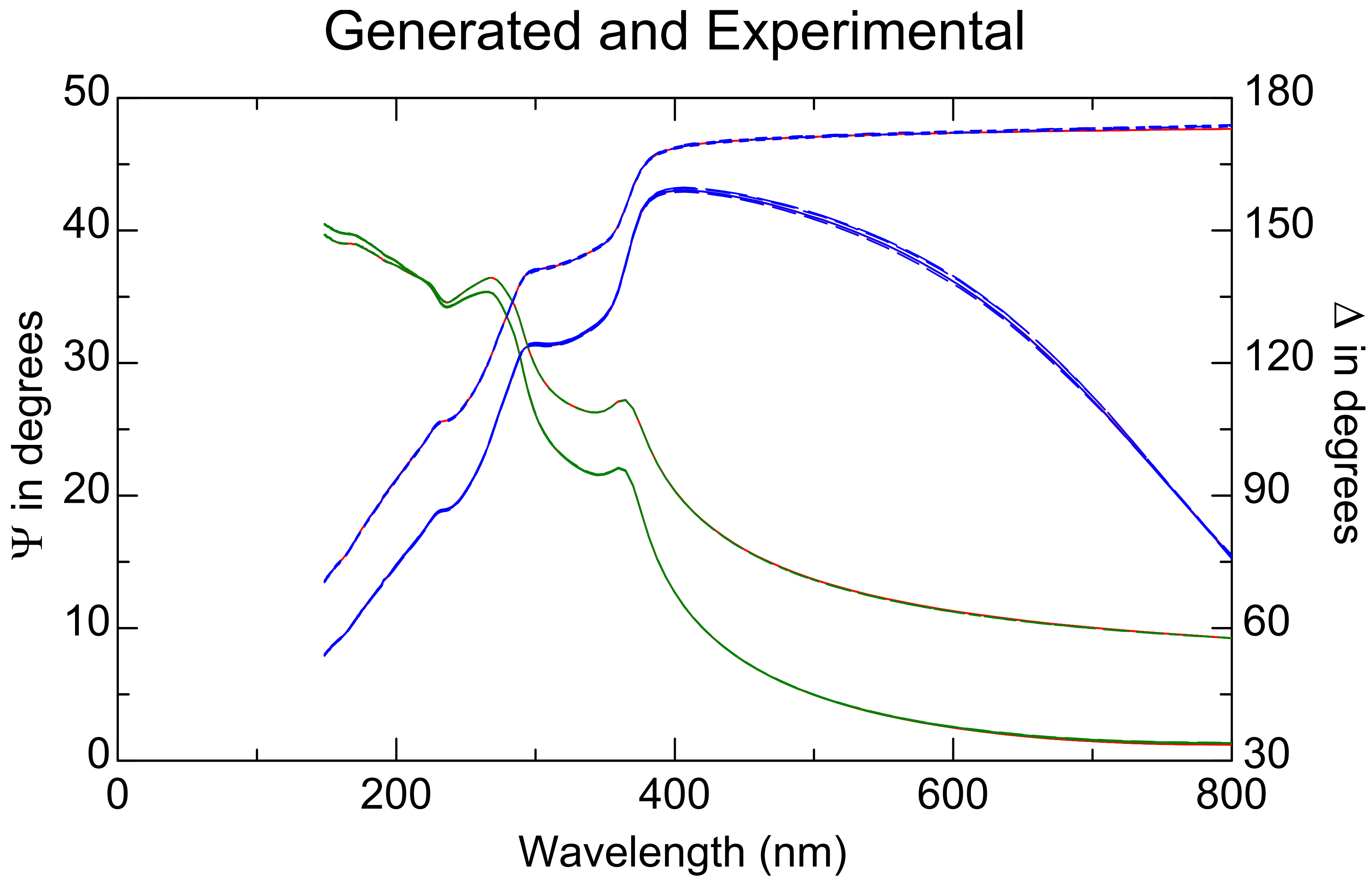
Hi-K/ oxide stack VASE™ results:



- **Rapid Thermal Oxide— independent of PDA**

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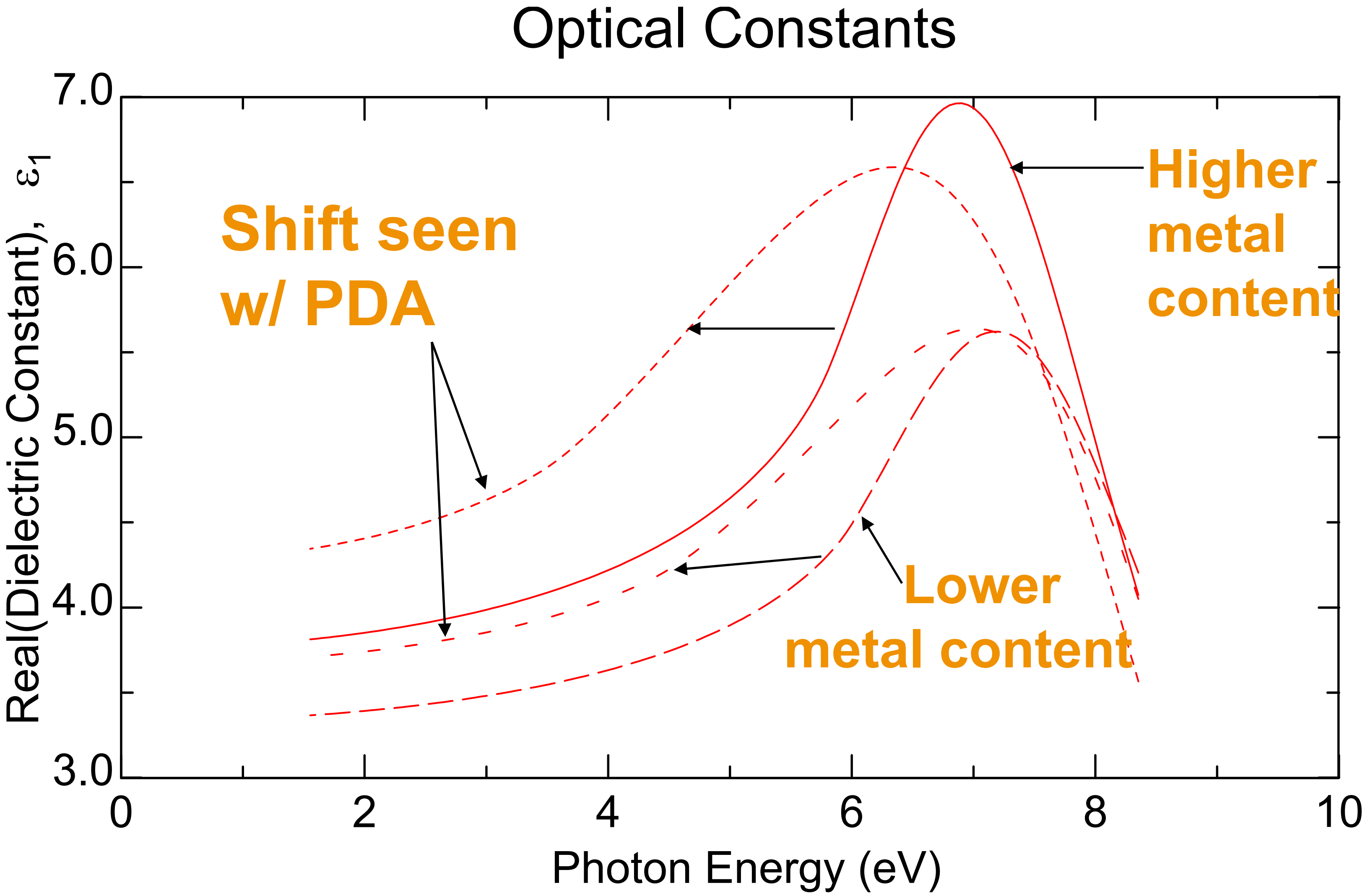
Hi-K/ oxide stack VASE™ results:

MOCVD High K silicates w/ post deposition anneal



Shift seen w/ PDA

Higher metal content

Lower metal content

Hi-K/ interfacial wafer calibration table:

Filmstack/ process info	T oxide [A]	T hi-K [A]	Index hi-K	MSE
Si/ interface/ hi-K #1	10.34	30.59	1.961	1.183
Si/ interface/ hi-K #1 (PDA)	12.43	24.26	2.097	0.8838
Si/ interface/ hi-K #2	5.84	25.67	1.841	0.9884
Si/ interface/ hi-K#2 (PDA)	6.68	26.61	1.933	1.59
Si/ oxide #1/ hi-K #1	24.94	24.97	1.961	0.6863
Si/ oxide #1/ hi-K #1 (PDA)	24.94	23.01	2.097	0.6827
Si/ oxide #2/ hi-K #1	26.02	23.86	1.961	0.6862
Si/ oxide #2/ hi-K #1 (PDA)	25.76	22.86	2.097	0.6806
Si/ oxide #1/ hi-K #2	21.84	24.25	1.841	0.6616
Si/ oxide #1/ hi-K #2 (PDA)	21.84	23.76	1.933	0.6595
Si/ oxide #2/ hi-K #2	22.8	25.72	1.841	0.6521
Si/ oxide #2/ hi-K #2 (PDA)	22.94	24.4	1.933	0.6563

High K/ interfacial layer optical metrology summary…

Standard spectroscopic ellipsometric approach parameters strongly coupled— not quite enough precision for interfacial layer thickness or material content

Approach also suffers from decreasing correlation with device characteristics— must account for process step induced changes present

Need to develop interface specific techniques

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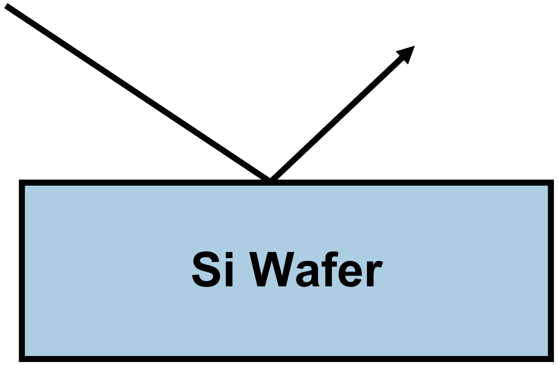
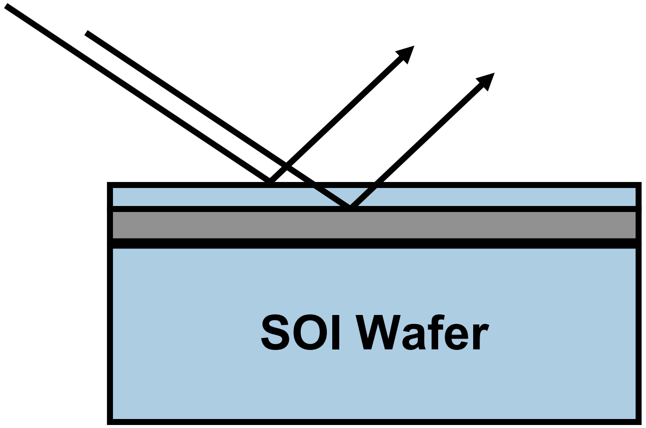
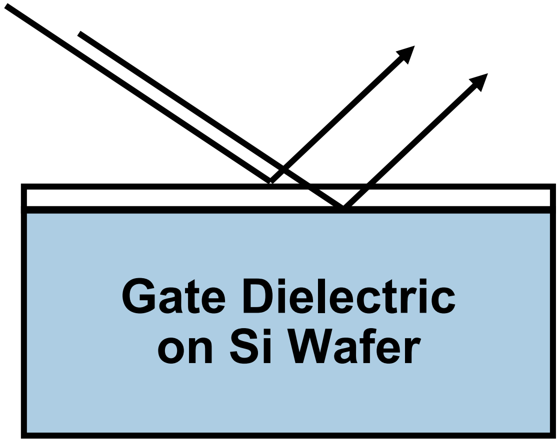
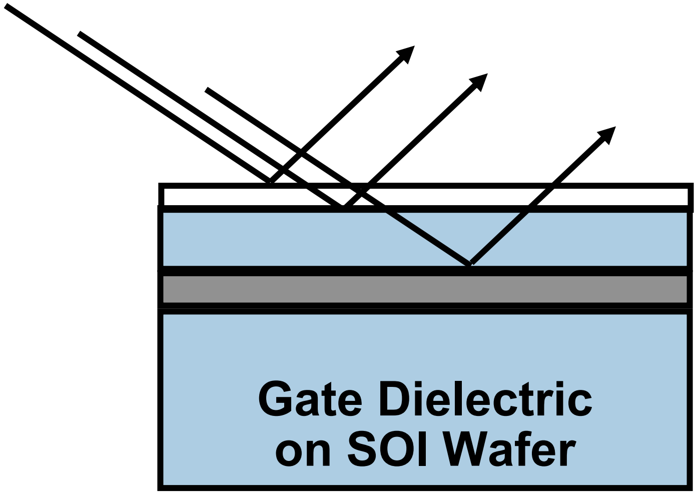
Extra reflection from SOI Wafers Impacts Ellipsometric Measurements

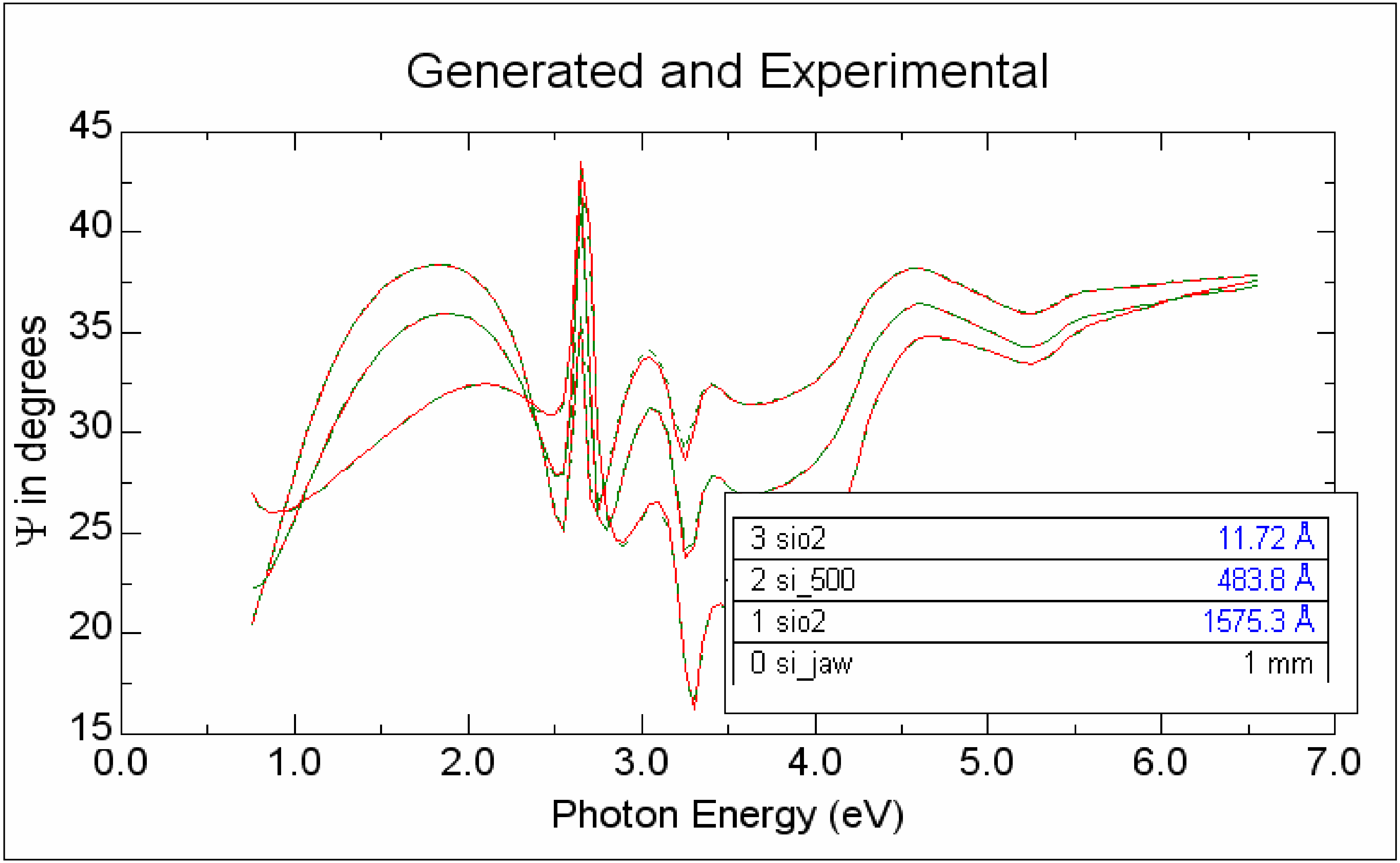








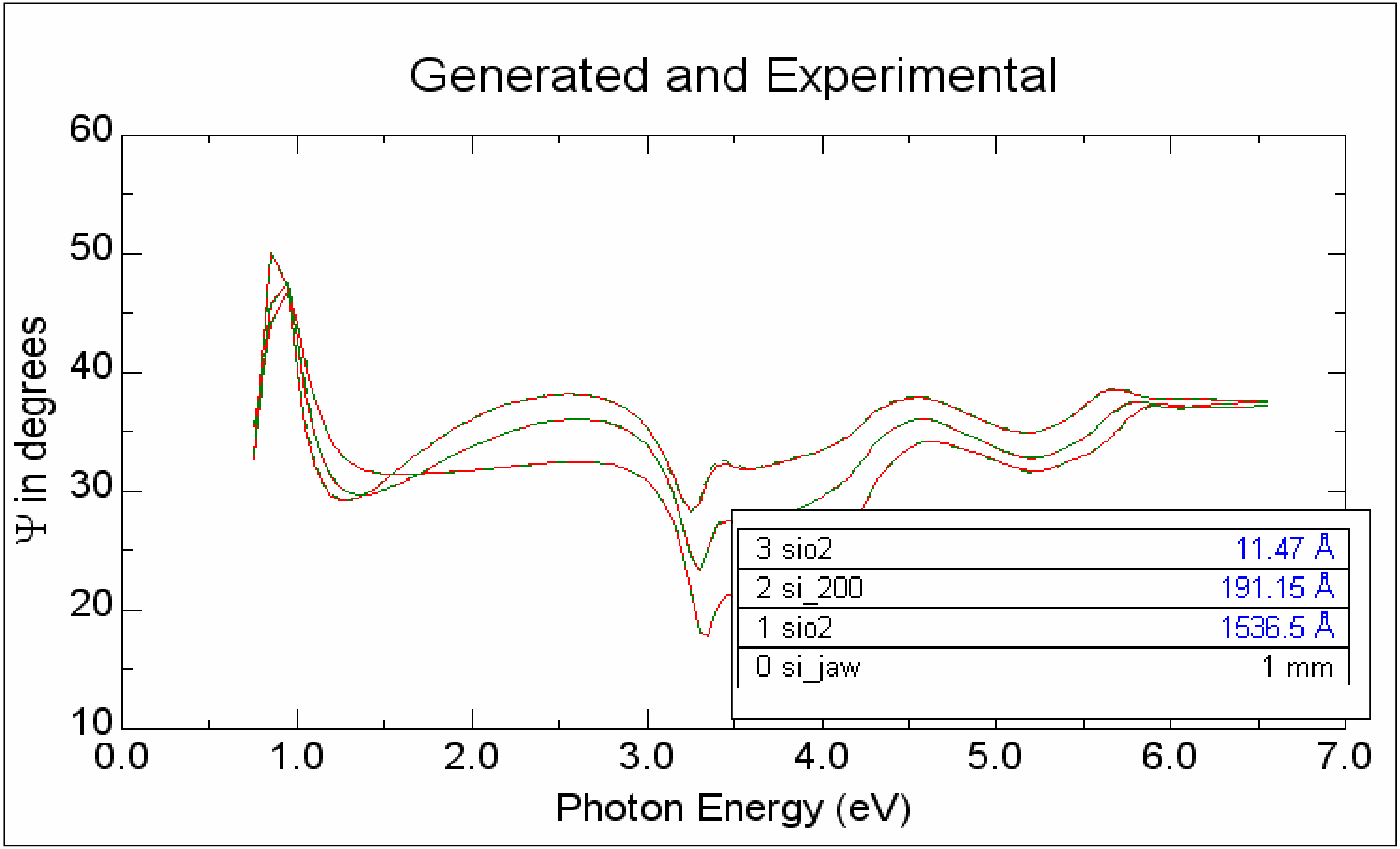
Optical models for Gate Oxide on SOI:



3 sio2	11.72 Å
2 si_500	483.8 Å
1 sio2	1575.3 Å
0 si_jaw	1 mm

Extra reflection may impact Gate Oxide on SOI precision

Optical models for Gate Oxide on SOI:



3 sio2	11.47 Å
2 si_200	191.15 Å
1 sio2	1536.5 Å
0 si_jaw	1 mm

MSE ~1.6 (~200A top Si)

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Gate Oxide on SOI substrate optical metrology summary…

Standard spectroscopic ellipsometric approach appears acceptable— excellent fitting seen, impact of extra-reflection needs evaluation

Future High K stack on strained SOI appears likely…

S. Zollner, et al., “Thin-film metrology of silicon-on-insulator materials”, Appl. Phys. Lett. vol. 76, 46 (2001).

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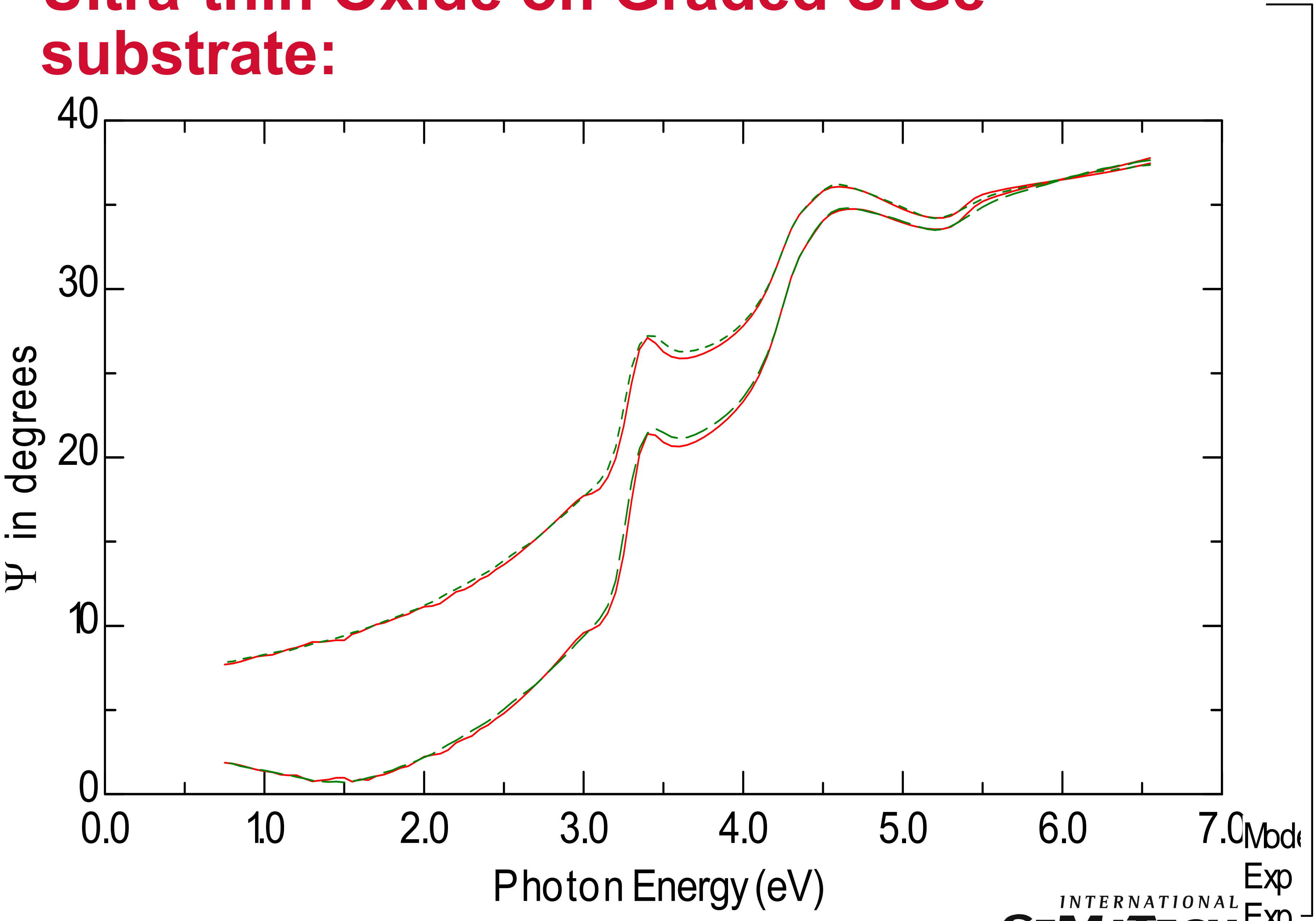
4. Future Gate Dielectric Metrology Challenges:

SE at limits- to characterize:

1. High K gate dielectric on Si substrate
2. High K/ interfacial oxide stack on Si
3. Gate Oxide on SOI
4. Gate Oxide on SiGe
5. Gate Oxide on SiGe-on-Insulator

Ultra-thin Oxide on Graded SiGe substrate:



Extraction of Graded SiGe layer thickness— wVASE™ results:

6	native oxide	0.00099613 µm
5	epi cap	0.012328 µm
4	sige x=0.920	2.6326 µm
3	sige graded si_jaw/ge	1.8177 µm
2	epi #2	0.16599 µm
1	epi	3.0234 µm
0	si substrate	1 mm

- **Increase in number of required parameters**

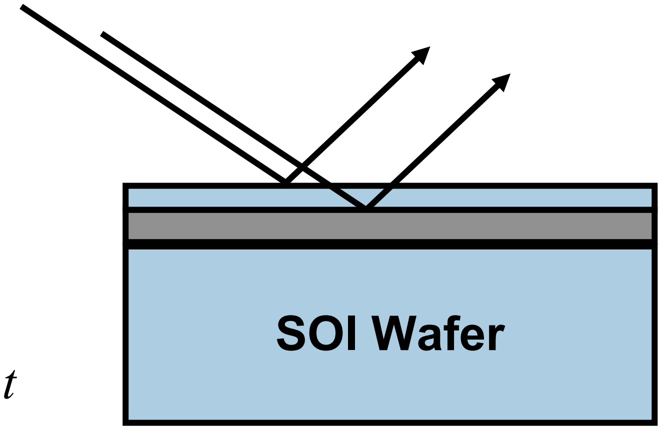
Timeline for Fully Depleted Ultra-thin body SOI–

115nm node (2002)	SOI ~16-27 nm	~~BOX ~40-66 nm~~
90nm node (2004)	SOI ~11-19 nm	~~BOX ~28-46 nm~~
65nm node (2007)	SOI ~8-13 nm	~~BOX ~19-31 nm~~
45nm node (2010)	SOI ~5-9 nm	~~BOX ~14-23 nm~~
32nm node (2013)	SOI ~4-7 nm	~~BOX ~10-16 nm~~
22nm node (2016)	SOI: 3-5 nm	~~BOX ~7-11 nm~~

BOX may stay at ~100nm

Ultra-thin Si layer has altered optical response:

1. Critical Point SHIFT:



$$E_{cp\,SOI} = E_{cp\,"bulk"} + \Delta E_{confinement}$$

$$\Delta E \cong \frac{\hbar^2\pi^2}{2m^*L^2} = \frac{h^2}{8m^*L^2} \cong \frac{(4.136\times10^{-15}eV\cdot s)^2}{8(m^*/m_e)(.511\times10^6 eV)L^2}\cdot\frac{(3\times10^8 m)^2}{s^2}$$

$m^* = 0.2m_e$, $L = 10$ nm $\Rightarrow \Delta E \cong .02$eV…

(fairly small)

However, if $L = 5$ nm $\Rightarrow \Delta E \cong .08$eV…

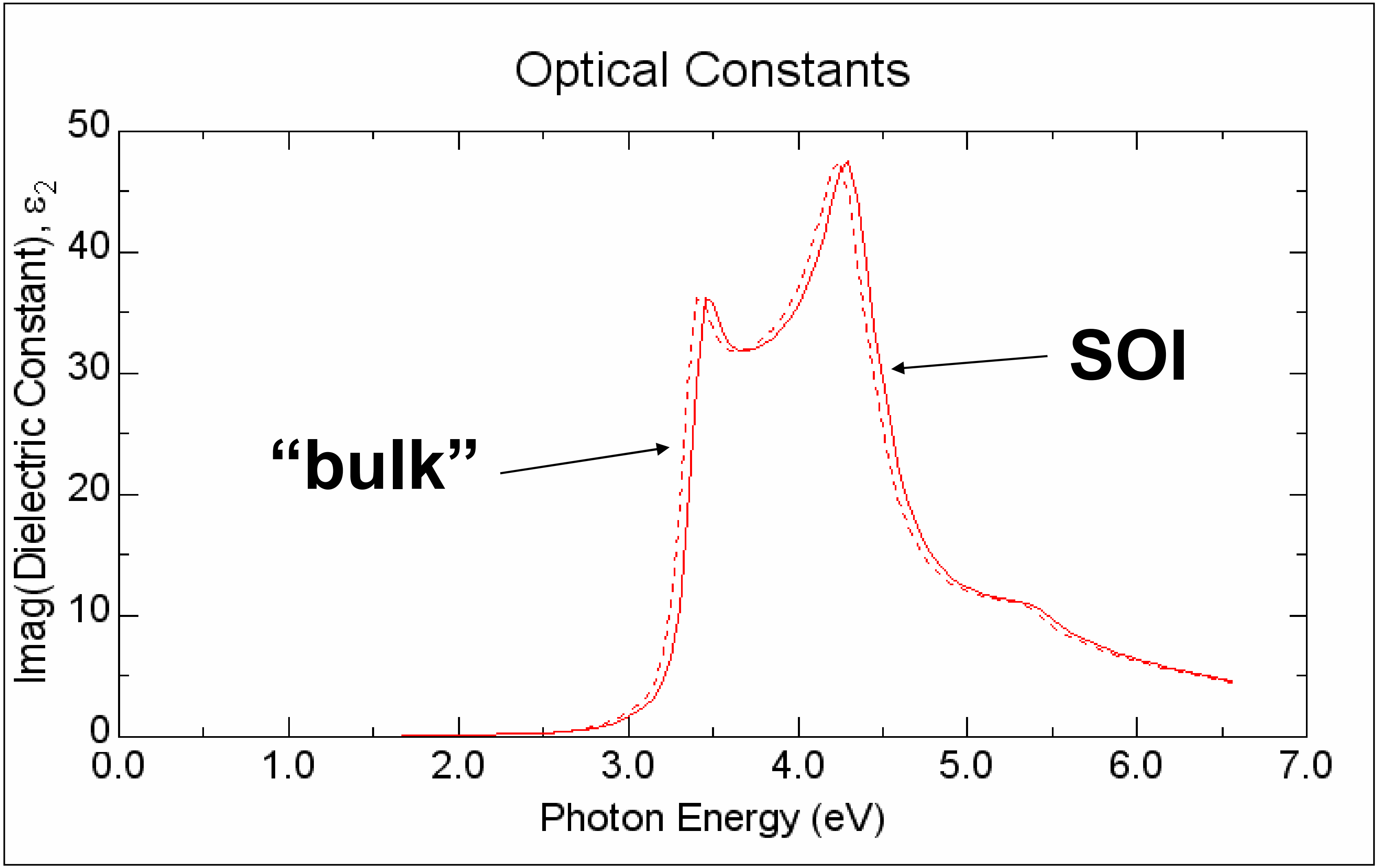
(becoming significant… shift scales as $1/L^2$)

Ultra-thin Si layer optical response (con’t):

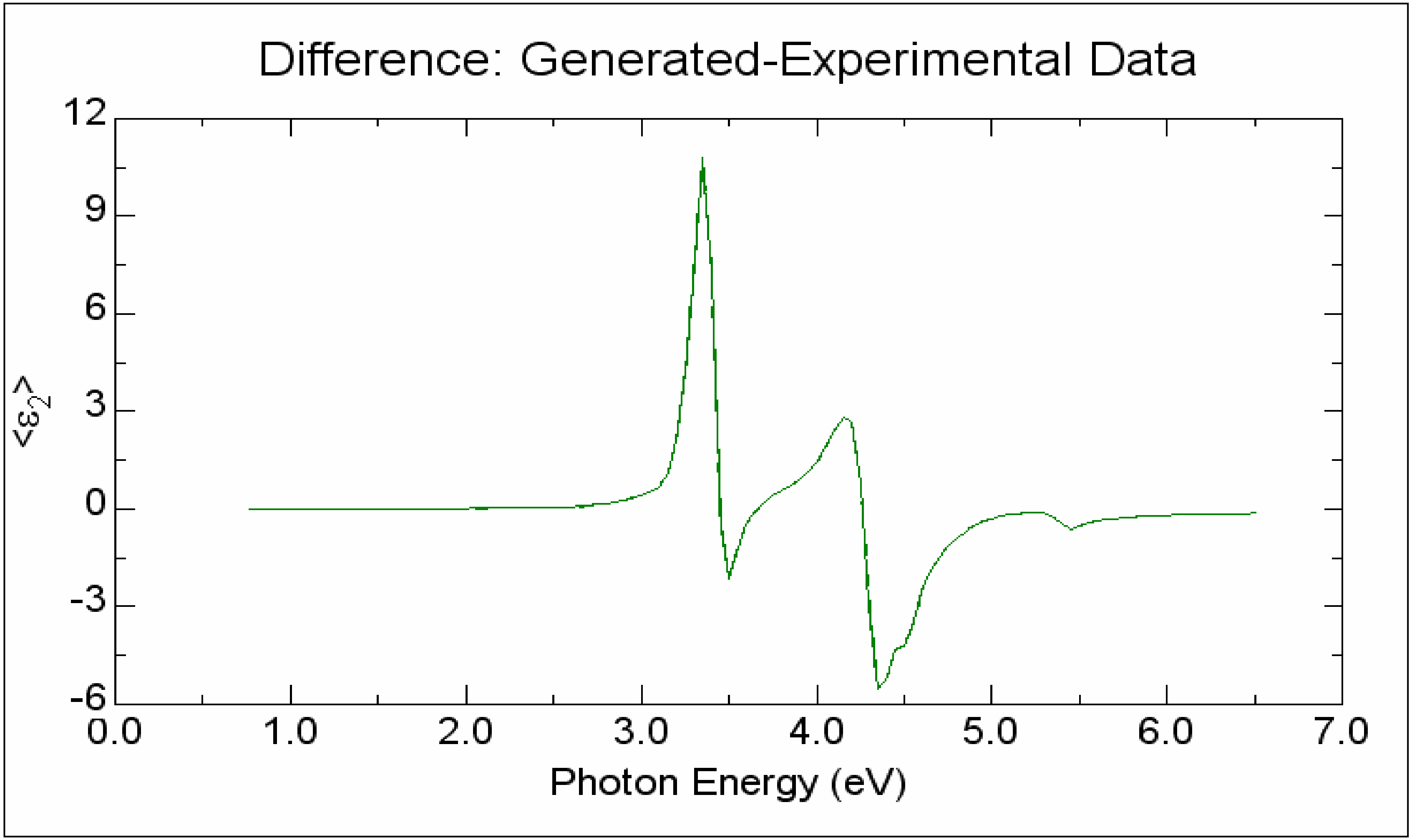
2. Critical point SHAPE:

DOS:	**Direct:**	**Indirect:**
“bulk”	$\varepsilon_2 \propto \frac{(\hbar\omega - E_g)^{1/2}}{\omega^2}$	$\varepsilon_2 \propto \frac{(\hbar\omega - E_g)^2}{\omega^2}$
“well”	$\varepsilon_2 \propto \frac{\Theta(\hbar\omega - E_g)}{\omega^2}$	$\varepsilon_2 \propto \frac{(\hbar\omega - E_g)^1}{\omega^2}$
“wire”	$\varepsilon_2 \propto \frac{(\hbar\omega - E_g)^{-1/2}}{\omega^2}$	$\varepsilon_2 \propto \frac{\Theta(\hbar\omega - E_g)}{\omega^2}$
	Describes $\Delta k_z = 0$ absorption, e.g. Si CP at ~3.3eV	**Describes $\Delta k_z \neq 0$ absorption, e.g. Si indirect band edge at ~1.1eV**

Schematic change in dielectric function of 5nm Si (no shape change):



Schematic difference in dielectric function of 50A Si (*vs*. “bulk”):



Biggest differences occur at structural features (CP shape change critical)

Extraction of Ultrathin body SOI optical response:

$$\varepsilon_2 \sim 1 = 2nk \qquad \alpha = \frac{4\pi k}{\lambda} \qquad \frac{I}{I_o} = \exp(-\alpha z)$$

$$\Delta\left\langle \varepsilon_2 \right\rangle \cong 1, n \cong 6.9, \lambda \cong 3760\ A, z \cong 50\ A$$

$$\frac{I}{I_o} \approx \exp\left\{-\frac{4\pi \cdot 50}{2 \cdot 6.9 \cdot 3760}\right\} \approx 99\%$$

⇒ Need ~1% differential intensity resolution, with resolution in photon energy of <.01eV, on a strongly absorbing background…

Future Gate Dielectric Metrology:

- Future gate stack projected to be High-K on SiGe-on-Insulator
- For High K/ oxide gate stack SE approach will need to be enhanced
- Optical Metrology for correlation to substrate characteristics may also be required

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… and many others